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REMARKS

This case has been carefully reviewed and analyzed in view of the Official Action dated 14 February 2002. Responsive to the rejections made in the Official Action, Claims 1-8 have been canceled by this Amendment and new Claims 9-19 have been inserted for further prosecution in this case.

In the Official Action, the Examiner objected to the entire disclosure as being replete with errors in form, grammar, spelling, and punctuation. Accordingly, the following changes to the disclosure are submitted herewith:

1. A supplemental copy of the original Application papers are enclosed herewith as per the Examiner's request. The supplemental Application papers are as originally filed, except that the lines of text are double-spaced, the text is printed on good quality paper, non-printable characters have been removed and non-English characters have been removed. The substantive content of the new Application papers is exactly that of the original Application, as filed.

2. The Title of the Invention, as originally filed, has been replaced with a brief but technically accurate and descriptive Title, "DIGITAL FM DEMODULATOR WITH REDUCED QUANTIZATION NOISE".

3. The Abstract, as originally filed, has been deleted in its entirety and

replaced by a Substitute Abstract to correct the numerous errors contained therein. It is believed that the Substitute Abstract now possesses proper form.

4. The Specification has been amended by replacement of the original Specification, as filed, with the Substitute Specification, which was the most efficient means to correct the numerous idiomatic, grammatical, and translational errors found therein. It is believed that the subject matter disclosed by the Substitute Specification was previously disclosed in the Specification and Claims, as filed, and the accompanying Drawing Figures. No new matter has been added by these changes. Additionally, a marked-up copy of the Supplemental Specification described above is attached to this Amendment in compliance with MPEP § 608.01(q). The Substitute Specification includes the same changes as are indicated in the marked-up copy of the Supplemental Specification.

In the Official Action, the Examiner rejected Claims 1, 2, and 4-8 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner found the Claims to be generally narrative and indefinite and containing numerous grammatical and idiomatic errors. As previously indicated, the original Claims, as filed, have been canceled by this Amendment and new Claims 9-19 have been

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inserted for further prosecution in this case. It is believed that the new Claims clearly and unambiguously define the metes and bounds of the instant invention, for which Patent protection is being sought.

The Examiner rejected Claims 1-8 under 35 U.S.C. § 102(b) as being anticipated by Hunsinger, et al. (U.S. Patent #5,465,396; hereinafter Hunsinger). The Examiner found that the reference discloses the method of operation of the invention of the subject Patent Application, as originally claimed.

Before discussing the prior art reference relied upon by the Examiner, it is believed beneficial to first briefly review the structure of the invention of the subject Patent Application. The invention of the subject Patent Application is a digital FM demodulator used in radio communication systems such as pagers, cellular phones, Global Positioning Satellite (GPS) systems, and Digital Enhanced Cordless Telecommunication (DECT) systems. The system utilizes a phase compensating feedback loop similar to that found in phase locked loops (PLL). The system also has elements and structure in common with Delta-Sigma analog-to-digital (A/D) converters to reduce quantization errors in producing the digital output sequence from a continuously-variable phase-proportional voltage level. The elimination of quantization error is especially imperative in the demodulation or decoding of digital signals in that the quantized error does not effect the output signal's

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amplitud[illegible] but rather places erroneous bit patterns into the digital time sequence. That is to say, th[illegible] a slight quantization error can cause a received bit to be in a logical "1" state when the[illegible] was originally transmitted in a logical "0" state.

A [illegible]dulated signal Ai containing digitally encoded information on an intermedi[illegible]e frequency (IF) signal is presented to the input of a segmented reference delay lin[illegible]which includes a course delay line for introducing a fixed delay into the input signal, an[illegible] fine delay line which is used to introduce a variable delay in discrete levels to the inp[illegible] signal. The fine delay line has coupled thereto a series of output taps, each of which are[illegible]nnected at the output of each of a series of discrete delay elements. The signal at[illegible]ch of the output taps is a delayed copy of the input signal, the delay time of each bei[illegible]the sum of the delay time of the course delay line and the sum of the delay time[illegible]s of[illegible]n fine delay element through which the output signal has passed up to the sel[illegible]ect[illegible]ut tap.

T[illegible]utput taps of the fine delay line are coupled to respective inputs of an M-to-1 multipl[illegible]. The multiplexer selectively couples one of the input terminals thereof to the outp[illegible]t[illegible]nal thereof such that the signal at the output of the multiplexer is a selected one[illegible]Ai[illegible]the delayed copies of the input signal taken from the fine delay line.

[illegible]yed signal Aid and input signal Ai are coupled to the input of a phase detector.

The phase detector produces an output pulse at its output port proportional in width to the phase difference between Ai and Aid. The output pulses of the phase detector are signed; they convey, by being either positive or negative, whether the signal Aid leads or lags the signal Ai.

The output port of the phase detector is coupled to a charge pump circuit, or charge integrator. The charge integrator produces a signal at its output proportional to an amount of stored charge accumulated therein. The storage of charge is controlled through the output pulses, received over time, from the phase detector. When the output pulse of the phase detector is positive, i.e., Aid leads Ai, charge is added to the charge accumulator and when the output pulse of the phase detector is negative, i.e., Ai leads Aid, charge is removed from the charge integrator. The output of the charge pump, Vf, increases and decreases according to the relative phase between Ai and Aid.

The output of the charge pump circuit is coupled to the input of a quantizer for producing the final digital output signal at the quantizer output terminal. Typically, the quantizer is an A/D converter. In the Delta-Sigma A/D converter configuration, as utilized in the subject digital FM demodulator, the quantizer is a 1-bit A/D converter or a voltage comparator. The quantizer converts Vf into a digital output sequence, y, by forming a change in state of the output signal when Vf crosses a reference voltage level.

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[illegible]dback mechanism is implemented through a digital integrator which takes at its input [illegible] digital output sequence y and produces at its output a binary delay selection wor[illegible] digital integrator may be a digital up/down counter which counts up when the sta[illegible]t signal y is a logical "1", and counts down when the output signal y is a logi[illegible]. The delay selection word at the output of the digital integrator is presented to the [illegible] port of the multiplexer to select one of the delayed input signals to present to the [illegible]tector circuit at the next cycle or sampling period.

[illegible]dvantage of the subject digital FM demodulator is that it requires no external cloc[illegible]iming reference. The components of the demodulator are synchronized th[illegible]modulated signal Ai. The output pulses of the phase detector are defined by the [illegible]ge of Ai and the rising edge of Aid. The charge in the charge integrator is ou[illegible] before the falling edge of Ai. The falling edge of Ai is optionally used to tri[illegible]uantizer and counter. This timing and its relationship to the frequency of the di[illegible]ut signal of the system realizes an inherent low pass digital filter in the de[illegible]r system. It is the inherent low pass filter that reduces the quantization noise in[illegible]y the quantizing process when producing the digital output sequence.

[illegible]tated hereinabove, the Examiner rejected Claims 1-8 under 35 U.S.C. § 102(b) as [illegible]ticipated by Hunsinger. Although the invention of Hunsinger is shown as

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have several elements in common with the subject digital FM modulator, important differences exist due to the nature of the output signal produced by each system. Hunsinger does not seek to extract a digital sequence and does not, therefore, recognize the problems associated therewith. Hunsinger's invention produces at its output an analog signal, i.e., one having a continuously variable amplitude which, if quantization error were to occur therein, only a minute deviation from an optimal amplitude would occur. In systems relying on analog signals for the conveyance of information, such errors in the reconstructed amplitude of a signal are unlikely to produce a catastrophic degradation in the information being transmitted. In the production of digital sequences, quantization errors result in incorrect data being inserted into the data stream, i.e., errors occur along the time axis. Errors of this type can render the information being conveyed undecipherable. Thus, the system of the present invention is designed to greatly reduce the occurrence of such errors.

As Hunsinger does not teach a digital demodulator, the reference does not show or suggest the use of a "quantizer configured to produce a digital output signal at an output terminal thereof" as implemented by the present invention, as now claimed. Furthermore, Hunsinger does not show or suggest the feedback structure of the present invention, i.e., "a digital integrator coupled to said digital output signal, wherein said digital integrator is

coupled to [a] multiplexer for selectively applying a delay". Only through the quantizer of the present invention is a digital output sequence produced and only through the feedback of the digital output sequence to select the appropriate delayed input signal for the next cycle is the inherent digital filter realized to reduce the quantization error of the quantizer. Hunsinger shows a process for controlling the digital delay through the phase detection process, not through feedback from the output signal. Whereas the feedback structure of the instant invention operates to minimize the phase difference detected by the phase detector, much like a PLL, Hunsinger's open-loop design does not. Hunsinger's objective is in providing the ability to cancel or filter out an undesired signal through a tracking delay element notch filter, which is adjusted continuously in response to the instantaneous frequency of a dominating interference signal (Column 6, Lines 26-58).

As previously stated, Hunsinger fails to disclose a "quantizer configured to produce a digital output signal at an output terminal thereof", nor "a digital integrator coupled to said digital output signal, wherein said digital integrator is coupled to [a] multiplexer for selectively applying a delay". Therefore, it is respectfully submitted that Hunsinger does not anticipate the invention of the subject Patent Application, as now claimed. Moreover, as Hunsinger does not show or suggest the combined elements for

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the purposes and objectives of producing a digital output sequence in the manner set forth in the subject Patent Applcation and as discussed hereinabove, it is submitted, respectfully, that the subject digital FM demodulator is not made obvious by the Hunsinger reference, either.

It is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being facsimile transmitted to Art Unit #2631 in the U.S. Patent and Trademark Office on the date shown below.

Date: 7/15/02

UP SUBSTITUTE ABSTRACT

ABSTRACT OF THE DISCLOSURE

A new ~~method of~~ digital FM demodulator ~~that~~ incorporates the concept of delta-sigma modulation to implement the function of time-to-digital converter. The FM demodulator is constructed from a multiplexer, a phase quantizer and a digital integrator. The modulated carrier passes through the delay lines, then the phase of the modulation signal is compared with the original input modulation signal and the comparison result is converted into a voltage and stored in a capacitor by way of charge accumulation. Meanwhile, the quantized voltage having been accumulated and quantized is acquired to compare its phase with the input signal. The phase difference between input signal and delayed signal is fed back to produce zero phase difference, much like a phase locked loop. In this manner, the digital signal is collected at the system output.

'KED-UP SUBSTITUTE SPECIFICATION

~~A New Method Of Digital FM Demodulator~~

FM DEMODULATOR WITH REDUCED QUANTIZATION NOISE

BACKGROUND OF THE INVENTION

1. Fi[illegible] ention
[illegible]ention

ivention relates to ~~a new method of~~ digital frequency-
dulation
nodulator and more particularly, to a digital ~~frequency~~ FM
extracts a digital time sequence from an intermediate
modulator that ~~using the structure of time-to-digital converter and~~
) carrier while reducing quantization error and eliminating
alta-sigma analog to digital converter~~
nt of a reference clock.

2. D[illegible] o The Prior Art

of information conveyance
cy modulation (FM) is ~~one of~~ an important and common method in
The of the system
ation system, ~~that its~~ receiver end contains the FM
is of
rcuit which often using analog design ~~circuit and the~~
a
~~alog-style FM demodulation circuit~~ including detector circuit and
is brought the a larger
/circuit. If ~~bring~~ the detector into integrated circuit, then ~~it need~~
the is built
and if ~~implement~~ PLL into integrated circuit, then an external
the the
essary outside ~~this~~ chip.
requires processing
ted signal ~~need the~~ digital signal ~~process~~ after
described above requires same
hen the ~~above two~~ circuit need analog-to-digital converter to
iod[illegible]ated analog signal into digital signal. ~~meanwhile, this~~ The
easily with To reduce noise
~~easy to be~~ interfered by noise ~~signal~~. However, the digital FM
modulated
ll first convert the ~~modulation~~ intermediate-frequency (IF) signal

necessary circuitry to implement an FM demodulator
-ted on an integrated circuit chip.

int[illegible]al by way of an analog-to-digital converter, then using digital signal
p[illegible]modulate this modulation signal. The analog-to-digital converter
a[illegible]al processor used in digital FM demodulator must have fast
s[illegible]dulate the modulation signal in real time. It also could use a
r[illegible]with multiple-fold frequency of modulation signal for sampling
t[illegible]lation signal to detect its phase change then demodulate, but
s[illegible]y need a high frequency reference clock.

[illegible]onal methods of digital RF communication system always need
t[illegible]nalog signal into digital signal in the receiver end with
[illegible]increasing the circuit complexity. Thus, the demodulation circuit
[illegible]tector circuit or PLL with analog-to-digital circuit could simply
[illegible]n also will be one of major objectives today.

[illegible]MARY OF THE INVENTION

[illegible]re a primary objective of the present invention to provide a new
[illegible]tal FM demodulator will be applicable in radio communication
[illegible]s, the modulation-demodulation section in receiver end also
[illegible]cable in BB call, cellular phone, GPS system, and DECT systems

[illegible]jective of the present invention is to provide a digital FM
[illegible]ith [illegible] function of modulation-demodulation and analog-to-digital

input intermediate-frequency signal passes through the inventive ~~this invention~~ generating a digital signal including a high-frequency quantization noise ~~quantized~~ way of a low-pass filter, ~~to filter out above~~ the quantized noise signal is filtered. ~~acqu~~ ~~t~~ band signal.

~~jective~~ of the present invention is to provide a digital FM ~~which adopt the~~ adapts a PLL structure and utilizes the concept of delta-~~sigma~~ conversion ~~-digital converter~~ does not require ~~which without connect~~ external components ~~or~~ reference clock, ~~so that easy for integration.~~

~~it~~ provides over similar systems in the prior art by using ~~with~~ advantages ~~that not only use~~ delay lines as the timing ~~adopting~~ ~~also~~ the concept of delta-sigma analog-to-digital conversion ~~converter~~ time-to-digital conversion ~~for~~ of digital FM demodulation ~~demodulator~~. This digital ~~in~~ ~~cles~~ ~~or~~ ~~ding~~ delay lines, an m-to-1 multiplexer, a phase e pump circuit, a quantizer and a digital integrator. The modulation ~~carrier~~ mediate frequency ~~segment~~ passes through the delay lines, each having a ~~with the~~ ~~the~~ phase of the is ~~and~~ with the ~~this~~ delayed signal compare its phase ~~co~~ ~~ison~~ produces a which is applied to the signal. ~~his~~ ~~compared~~ pulse ~~will go through~~ charge pump circuit where ~~e~~ charge is ~~to a voltage level~~ stored in a capacitor. This quantized voltage is charge is into a level which by the digital integrator, then a new sample of another output signal of the ~~d~~ in ~~nd~~ compare phase with the input signal. This system is similar to a PLL, i.e., ~~y~~ phase as the error signal ~~system~~. The quantized digital signal will feed through the low-pass

def the sampling rate of the system

ut high frequency noise and get the original modulation signal, i.e.,

n signal is the output a digital signal.

BRIEF DESCRIPTION OF THE DRAWINGS

gs disclose an illustrative embodiment of the present invention,

to exemplify the various advantages and objects thereof, and are

ircuit block diagram of the digital FM demodulator according to the

ntion.

ircuit waveform of the digital FM demodulator according to the present

system structure of the digital FM demodulator according to the present

LED DESCRIPTION OF THE PREFERRED EMBODIMENT

refer to Fig.1 that relates to the circuit block diagram of digital FM
ator. The modulation signal, Ai(t), is fed into reference delay lines 11,
ence delay lines 11 including coarse delay line 111 and fine delay line
lay time of delay lines 111 and 112 is controlled separately by
cuits. The fine delay lines 112 has multiple output signals
?(t),Ai3(t)..... Aij(t) which could be expressed as follow:
-Tc "T) —(1)
ed delay time of coarse delay lines, and
it delay time of fine delay lines.

tector compares the phase difference between Aid and Ai,then
down signal. The m-to-1 multiplexer will select one of output
0(t) i1(t),Ai2(t)..... Aij(t) from fine delay lines 112 and name it as Aid
he rising edge of Aid signal lead the Ai signal, up signal will generate as
ve e, and its pulse width is just same as the time difference
g edges of Ai and Aid, but down signal do not genarate any
The total delay time of Ai signal pass through delay lines is
he pulse width will equal to "T-Tc-d*T" when "Tc+d*T" smaller
signal.
if the rising edge of Aid signal lag the Ai signal, down signal
effective pulse and its pulse width is also just same as the time
and Ai signal, and the pulse width will equal to "Tc+d*T-T".

Which illustrates the
modulation
are
have
13
then
delayed signals,
the
be
having a
equivalent to
and then will not be generated
impressed on the by pass since, the
where d is the number of fine delay lines and
similarly
a
having
equal to
i.e.,
be
to

The pl

put

itive when Aid lead the Ai signal, ~~on the contrary~~, while its value is considered
lag the signal. ~~Both effective~~ The pulse of the up and down signals will are applied

pump circuit 14 for charging and discharging a capacitor, Cc,
a voltage difference, Vf, ~~and its~~ the voltage level of which is proportional
nce or phase difference of the Aid and Ai signals.
input
odulated signal will generate a Vf which is accumulated
or Cc, ~~and this~~ the stored voltage will be quantized by quantizer 15 to generate a bit
nal y(k), ~~y(k)~~ which is the output digital sequence of the total system.
s a analog-to-digital converter which may be ~~could be one-~~ bit or
erter, one-bit converter ~~is the~~ may be implemented by a voltage
comparator. The quantizer 15 ~~is~~ is a
In the preferred embodiment,
opt one-bit voltage comparator.
In the preferred embodiment,
tor 16 accumulate the output digital signal y(k), ~~actually, it is simply~~
aking the output of as its input
ter ~~to~~ quantizer 15 ~~is one bit analog-digital converter~~. The

digital rule

ignal will select one output Aid signal from the fine delay lines
12
plexer ~~and compare its phase with Ai signal~~. ~~Consequently~~, Thus the
The applied will be increased by
d sign is controlled by output signal y(k), ~~it will~~ delay one ~~more~~
Conversely
1. ~~On the contrary~~, the delay of Aid will decrease one unit delay if
functions
is whe system is similar to a PLL structure. The output signal y(k) fed back
~~y(k)~~ is ~~feedback~~ to

delay time and make the next rising edge of Ai signal arrive at
simultaneously with the
with ing edge of Aid ~~signal simultaneously~~. so the Aid signal
of the
one cy than Ai signal when the system is locked.

to the
n in Fig.2, this is the circuit waveform of digital FM demodulator
are shown the modulated
o the present invention, T(k) is the kth cycle time of input modulation
the rising edge of and the
P(k) is the time difference of Aid rising edge with next Ai cycle. The
the a and
ulse of up signal means P(k) is positive value, but the down signal
) negative. That is because the maximum frequency shift of input
n signal is much smaller than carrier frequency, the change of T(k) is
Tc
ive to carrier cycle Tc.
the
re, the effective pulse of up signal and down signal only happen at the
the
e of Aid and Ai signal and this effective pulse has been transferred to
15
storage
stored in capacitor Cc by way of charge pump circuit before arriving of
14 the arrival of the
The of Ai used as 15
ge. This falling edge could be the trigger clock of the quantizer and
Thus, the does not require an IP using the
eans this system do not need external reference clock. As shown in
of Fig.2 may be developed
veform diagram, a formula as follows :

?(k)+T(k)-T(k-1)+y(k)*T, ——(2)

P where

(k)-T(k-1), ——(3)

e, we could get

?(k)+ ΔT(k)+ y(k)*T, ——(4)

the as shown in
15
) means the capacitor voltage at kth cycle based on Fig.2, we could
an
) signal is generated by V(k-1) and Ic signal to charge/discharge Cc

up or down signal effective pulse period and Ib charge/discharge Cc to

h cycle, i.e. the voltage is determined by these three parameters. those

age on Cc for Ic at kth cycle is :

Ic/Cc*P(k) —— (5),

trigger clock is the input modulation signal Ai, then the Cc voltage level change in the

next formula when charge-discharge is at kth cycle, the will be

y(k)*Ib/Cc*[T(k)+T(k+1)]/2 —— (6),

Vf_a+ΔVf_b —— (7)

V(k)+{y(k)*(Ib/Cc)*[T(k)+T(k+1)]/2}+{Ic/Cc*P(k)} —— (8)

ause the maximum frequency shift is much smaller than carrier

cy, the T(k) is around approximately equal to carrier cycle Tc and

=V(k)+Ic/Cc*P(k)+y(k)*(Ib/Cc)*Tc —— (9)

e

and

Cc)*Tc. Then

ld get next formula ?

=V(k)+A*P(k+1)+B*y(k).

In P(k+1) into above formula, then we get

$V^{n+1}=V(k)+A*[P(k)+\Delta T(k)+y(k)*\tau]+B*y(k)$

The quantized output of V(k), y(k), is the total system output.

[illegible]ring to
[illegible]own in Fig.3, is the system structure of digital FM demodulator
[illegible]ng to the present invention. This diagram is a two level delta-sigma
[illegible]ct[illegible] its input is ΔT(k), that also is the signal difference of T(k) and T(k-1).
[illegible]oncept of the output signal y(k) in present invention is similar to
[illegible]ional analog-digital converter output signal. the quantized noise signal
[illegible]s high frequency segment. So the output digital signal y(k) is
[illegible]ated first then filter out quantized noise by the digital filter to get the
[illegible]ion signal.
[illegible]technology is similar to conventional delta-sigma analog-to-digital
[illegible] Based on above deduction, the output digital signal is produced by
[illegible]iation of original modulation signal. In brief, y(k) signal filter out the
[illegible]d noise by way of low-pass digital filter before signal accumulation.

[illegible]nvention provide a FM digital demodulator which with more advantages
[illegible]ventional technology as follow:

1. ethod and circuit in present invention will be applicable in radio
nication system, besides, the modulation-demodulation section in a
er and also could be applicable in BB cell, cellular phone, GPS system,
and ECT system.

2. esent invention to provide a digital modulation demodulator which
a
the PLL structure and utilize the concept of delta-sigma analog-to-
dig converter which without connect external component and high
ncy reference clock so that easy for integration.

3. esent invention to provide a digital modulation demodulator with two
of demodulation and analog-to-digital conversion. The input of
ediate-frequency signal pass through this invention demodulator will
ate a digital signal including high-frequency quantized signal, then by
low-pass filter, to filter out above quantized noise signal to get the
band signal.

changes and modifications in the above described embodiment of the
can, of course, be carried out without departing from the scope
ccordingly, to promote the progress in science and the useful arts, the
n is disclosed and is intended to be limited only by the scope of the
d claims.